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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	
Guy L. STEELE, Jr.	Group Art Unit: 2193
Application No.: 10/035,747	Examiner: Mai, Tan V
Filed: December 28, 2001	
For: FLOATING POINT SYSTEM THAT REPRESENTS STATUS FLAG INFORMATION WITHIN A FLOATING POINT OPERAND	Confirmation No.: 3637

Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY BRIEF

Pursuant to the provisions of 37 C.F.R. § 41.41 and M.P.E.P. § 1207.03(V), Appellant requests that this appeal be maintained, for the reasons set forth in this Reply Brief, filed in response to the Examiner's Answer mailed December 27, 2006. This Reply Brief is being timely filed within two months of the Examiner's Answer.

If any fees are required, Appellant requests that the required fees be charged to Deposit Account No. 06-0916.

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I. STATUS OF CLAIMS

Claims 1-54 remain pending, under current examination, and subject to this appeal.

II. GROUNDS OF REJECTION TO BE REVIEWED

A. Claims 1-54 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,995,991 to Huang et al. ("Huang"), as modified by the Examiner's Answer. Examiner's Answer at 3. Appellant appeals this rejection of those claims.

B. Claims 1-54 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,009,551 to Lynch et al. ("Lynch"), as modified by the Examiner's Answer. Examiner's Answer at 3. Appellant appeals this rejection of those claims.

III. ARGUMENT

This Reply Brief supplements the Appeal Brief filed April 7, 2006 by responding to the Examiner's Answer mailed December 27, 2006 that included new grounds of rejection. This Reply Brief responds to the Examiner's new arguments, where appropriate, and to the new rejections in the Examiner's Answer.

A. Reply to the Examiner's modified rejection of claims 1-54 under 35 U.S.C. § 102(b) as being anticipated by *Huang*

With respect to claim 1, as best understood by Appellant, the Examiner alleges that Huang's X register 116 (Fig. 4) constitutes the claimed "operand data structure," that Huang's X operand portion 116-1 constitutes the claimed "floating point operand data," and that Huang's X_tag 116-2 constitutes the claimed "embedded status information." Examiner's Answer at 26. These allegations are incorrect. Stated simply, a register is not an "operand data structure," as recited by claim 1. A register is hardware—a device that stores information. In contrast, an operand data structure is a software organization of data, such as an array, a linked list, a stack, or in this case, a unique operand having embedded status information.

Dependent claim 2 recites determining "at least one status condition" from "the embedded status information without regard to memory storage external to the data structure" (emphasis added). In the Examiner's Answer, the Examiner asserts: "Huang's tag (x_tag) [116-1] . . . is a portion of X operand register 116." Examiner's Answer at 26. But as discussed above, a register is not an operand data structure. Moreover, even assuming Huang's X operand portion 116-1 could be construed as an operand data structure, Huang's x_tag 116-2 is separate and external to operand

portion 116-1. Huang, Fig. 4. Therefore, Huang's x_tag 116-2 (alleged embedded status information) is not be embedded within operand portion 116-1 because Huang both illustrates and describes operand portion 116-1 and x_tag 116-2 as being separate.

The Examiner's allegation regarding claim 3 in the Examiner's Answer is not clear. The Examiner states "It is noted that the phrase 'without regard to memory storage external to the data structure' in parent claim [2] implied the embedded status information is not associated with data from the memory storage external like Appellant's Fig. 1 (PRIOR ART, FLOATING POINT STATUS REGISTER 25)." Examiner's Answer at 27 (emphasis in original). The Examiner then concludes "Therefore, Huang's tag (x-tag) 166-1 [sic] is the same as the claimed features." Id. It is not clear how these statements relate to the specific claim elements. Huang's x_tag 116-2 (alleged status information) is contained within register 116 (the alleged floating point status register). This is exactly opposite to the claimed "[at least one status condition . . . without regard to] a floating point status register," as recited in claim 3.

In the Examiner's Answer, the Examiner provided a new rejection of claims 6-15 under 35 U.S.C. § 102(b) as being anticipated by Huang. The Examiner summarily rejected these claims, alleging: "The claimed formats are inherent features in the floating point operands in Huang. The status and flags are disclosed in col. 1 lines 55-60, col. 7 lines 20-23 and table 1 in col. 6 of the Huang patent." Examiner's Answer at 5. This is not correct. Although the Examiner has repeatedly lumped these claims together, each claim recites unique and varying elements that patentably distinguish from Huang. For example, Huang does not teach or suggest an "overflow status [that]

represents one in a group of a +OV status and a –OV status," as recited by claim 6; an "overflow status . . . represented as a predetermined non-infinity numerical value," as recited by claim 7; an "underflow status [that] represents one in a group of a +UV status and a – UV status," as recited by claim 8; an "underflow status [] represented as a predetermined non-zero numerical value," as recited by claim 9; or "at least one status condition [] associated with at least one floating point operation that generated the enhanced floating point operand data structure," as recited by claim 15.

Moreover, M.P.E.P. § 2112 instructs: "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic" (emphasis in original). Rather, "the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Id. (emphasis in original). The Examiner has not provided any basis in fact or technical reasoning to support his general allegation that the claimed elements are inherent in the disclosure Huang. Accordingly, the Examiner's reliance on inherency is improper and the rejection of claims 6-15 should be withdrawn.

In the Examiner's Answer, the Examiner provided a new grounds of rejection for claims 16-20 under 35 U.S.C. § 102(b) as being anticipated by Huang. Claim 16 recites "a floating point operand data structure" having a "first data field," "second data field," and "third data field." The Examiner alleged: "the claims are similar to claims 1-15 except the independent claim 16 adds the 'floating point operand data' having 'sign', 'exponent' and 'fraction' information." Examiner's Answer at 5. The Examiner alleges Huang's res_sgn constitutes the claimed "sign", Huang's res_exp constitutes the

claimed "exponent", and Huang's res_mag constitutes the claimed "fraction". Id. The Examiner's general allegation that claim 16 is "similar to" claim 1 indicates the Examiner's failure to address each and every element recited by the claims.

Rather, claim 16 even further distinguishes from Huang. As discussed above, Huang's register 116 is not an "operand data structure." Moreover, Huang's register only has two portions—116-1 and 116-2, not a "first data field", a "second data field", and "a third data field," as claimed.

Moreover, the Examiner has not address the claimed "wherein at least one of the first data field, the second data field and the third data field further includes embedded status information associated with at least one operand status condition" (emphasis added). Huang's Fig. 4, cited by the Examiner, illustrates that the res_sgn, res_exp, and res_mag are output from arithmetic section 114. s

The rejection of claims 17-20 under § 102 as anticipated by Huang is incorrect for the same reasons set forth in Appellant's appeal brief in response to the previous rejection of claims 17-20 under § 103 based on Huang, in which Appellants specifically pointed out the elements of claims 17-20 which are not taught by Huang.

In the Examiner's Answer, the Examiner alleges with respect to claims 21-31: "the examiner believes that the storing status information 'tag value' within the processed floating point operand." Examiner's Answer at 27. This new allegation cannot be understood. The Examiner also newly alleges that a format of stored data "in the MEMORY (REGISTER FILE) 112 is the **same as** the format [status data within the floating point operand] of **data transferred** to 'X' operand register 116 . . . ." Id.

(emphasis in original). Again, this new allegation cannot be understood. Claim 21 contains no recitation of a "format".

Moreover, in the Examiner's Answer, the Examiner concedes that Huang does not teach or suggest the claimed "control unit" (Examiner's Answer at 27). This admission, by itself, establishes that the rejection of claims 21-31 under 35 U.S.C. § 102 is improper. The Examiner references Appellant's FIG. 1. If the Examiner is making an attempt to combine Huang and Appellant's Fig. 1 (assuming arguendo Appellant's Fig. 1 is prior art), the rejection would only be proper under 35 U.S.C. § 103(a), and the Examiner would have to provide motivation to combine the references. And even then, the Examiner's assertion that Appellant's Fig. 1 "should have" the claimed elements does not support a rejection under 35 U.S.C. §§ 102 or 103.

In the Examiner's Answer, the Examiner provided a new rejection of claim 32 under 35 U.S.C. § 102 as being anticipated by Huang. The Examiner alleges: "Huang et al.s [sic] special operand generator 122 corresponds to the additional functional unit as claimed." Examiner's Answer at 5. This is not correct. Huang's operand generator 122 neither "concurrently process[es] an additional floating point operand," nor "stor[es] status information related to the additional floating point operand within the additional floating point operand while the status information related to the other floating point operand is preserved within the other floating point operand," as recited by claim 32.

B. Reply to the Examiner's modified rejection of claims 1-54 under 35 U.S.C. § 102(b) as being anticipated by *Lynch*

In the Examiner's Answer, the Examiner appears to allege with respect to claim 1 that Lynch's register stack is an "operand data structure". Examiner's Answer at 29.

Similar to the discussion of the rejection based on Huang above, (1) a register stack is not an "operand data structure," (2) Lynch does not teach or suggest the claimed "embedded status information," and (3) Lynch suffers from the same drawbacks of the prior art discussed in Appellant's specification.

Regarding claim 2, the Examiner's Answer at 29 now cites to the Abstract of Lynch for allegedly disclosing the claimed determining "at least one status condition" from "the embedded status information without regard to memory storage external to the data structure" (emphasis added). But as discussed above, a hardware register is not an operand data structure. Moreover, even assuming Lynch's register stack were an operand data structure, Lynch's tag field 89 is clearly separate and external to reg field 87, and not "embedded status information" within the data structure, as recited by claim 1.

The Examiner's new allegation regarding claim 3 in the Examiner's Answer at 29-30 cannot be understood. The Examiner mentions Appellant's Fig. 1 and then concludes "Therefore, Lynch's Tag Field 89 is the same as the claimed features." Examiner's Answer at 30. Nevertheless, claim 3 recites determining "[at least one status condition . . . without regard to] a floating point status register." Lynch's register stack containing the tag field 89, alleged status information, is the opposite disclosure of determining a status condition without regard to "a floating point status register," as recited by claim 3.

In the Examiner's Answer, the Examiner provided a new rejection of claims 6-15 under 35 U.S.C. § 102(b) as being anticipated by Lynch. The Examiner summarily rejected these claims, alleging: "These features are inherent in the special floating point

number in Lynch (see e.g. Fig. 5)." Examiner's Answer at 6. This is not correct. Although the Examiner has lumped these claims together, each claim recites unique and varying elements that patentably distinguish from Lynch. For example, Lynch does not teach or suggest an "overflow status [that] represents one in a group of a +OV status and a –OV status," as recited by claim 6, an "overflow status . . . represented as a predetermined non-infinity numerical value," as recited by claim 7, an "underflow status [that] represents one in a group of a +UV status and a – UV status," as recited by claim 8, an "underflow status [] represented as a predetermined non-zero numerical value," as recited by claim 9, or "at least one status condition [] associated with at least one floating point operation that generated the enhanced floating point operand data structure," as recited by claim 15.

Again, the Examiner provides absolutely no basis for an allegation of inherency, as discussed above with respect to the rejection of claims 6-15 under 35 U.S.C. § 102 as being anticipated by Huang.

In the Examiner's Answer, the Examiner provided a new grounds of rejection for claims 16-20 under 35 U.S.C. § 102(b) as being anticipated by Lynch. The Examiner alleged: "the claims are similar to claims 1-15 except the independent claim 16 adds the 'floating point operand data' having 'sign', 'exponent' and 'fraction' information. Lynch et al's device is a floating point device, therefore these features are inherent in the floating point operands in Lynch." Examiner's Answer at 6. Again, the Examiner's unsupported reliance on inherency is not proper and does not support a rejection under 35 U.S.C. § 102.

Moreover, independent claim 16 even further distinguishes from Lynch. Claim 16 recites "a floating point operand data structure" having a "first data field," "second data field," and "third data field." As discussed above, Lynch's hardware register stack 84 is not an "operand data structure." Moreover, Lynch's register stack 84 only has two portions—87 and 89, not first, second, and third portions as claimed. Furthermore, the Examiner has not shown how the cited reference allegedly teaches the claimed "wherein at least one of the first data field, the second data field and the third data field further includes embedded status information associated with at least one operand status condition," of claim 16 (emphasis added).

In the Examiner's Answer, the Examiner alleges with respect to claims 21-31: "the examiner interprets the floating point register as a operand . . ." Examiner's Answer at 30. As discussed above, a hardware register is not an operand. Moreover, in the Examiner's Answer, the Examiner concedes that Lynch does not teach or suggest the claimed "control unit" (Examiner's Answer at 30). Once again, this admission, by itself, establishes that the rejection under 35 U.S.C. § 102 is improper. Even further, the Examiner again improperly relies on inherency without any support or technical explanation. Id.

In the Examiner's Answer, the Examiner provided a new rejection of claim 32 under 35 U.S.C. § 102 as being anticipated by Lynch. The Examiner alleges: "Lynch discloses a Reorder Buffer corresponding to the claimed additional function unit." Examiner's Answer at 6. This is not correct. Lynch's reorder buffer neither "concurrently process[es] an additional floating point operand," nor "stor[es] status information related to the additional floating point operand within the additional floating

point operand while the status information related to the other floating point operand is preserved within the other floating point operand," as recited by claim 32.

IV. Conclusion

For the additional reasons given above, supplementing those presented in the Appeal Brief filed on April 7, 2006, pending claims 1-54 are allowable. Appellant respectfully requests that the Board reverse the Examiner's rejections.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Reply Brief, Appellant requests such an extension. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 20, 2007

By: _____
Nathan A. Sloan
Reg. No. 56,249